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FOR

# BROADBAND INTEGRATED DIGITALLY TUNABLE FILTERS

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# BROADBAND INTEGRATED DIGITALLY TUNABLE FILTERS

## FIELD OF THE INVENTION

**[0001]** This invention relates generally to tunable filters.

## BACKGROUND OF THE INVENTION

**[0002]** Tunable receivers used in cable television set-top boxes and in other applications receive broadband signals having many channels. It is a function of such a tunable receiver to produce the signals in a desired channel and reject the signals in the remaining channels. In rejecting the signals in the undesired channels, the tunable receiver should substantially remove all signals associated with the undesired channels so that the receiver outputs substantially the signals in the desired channel. These unwanted signals include image, harmonics, spurious, and other undesired signals.

**[0003]** Both single conversion and double conversion receivers are known in the prior art. In a single conversion receiver, the RF signal is directly down converted to the desired frequency range, either to an intermediate frequency (IF) or sometimes to baseband. In a double conversion receiver, two frequency conversions are used. Usually the selected channel is up shifted in frequency to a fixed frequency, and then down shifted from that frequency to a fixed IF frequency. In either case, various circuits with differing degrees of integration are known for the purpose. However, such circuits require, among other things, a way of changing the frequency selectivity of at least one filter circuit for channel selection purposes, as do other RF and many other circuits.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0004]** Figure 1 illustrates a block diagram of an exemplary prior art tunable receiver;

**[0005]** Figure 2 illustrates a block diagram of an exemplary tunable receiver in accordance with an embodiment of the invention;

**[0006]** Figure 3 illustrates a schematic diagram of an exemplary tracking filter in accordance with another embodiment of the invention;

**[0007]** Figure 4 illustrates a schematic diagram of an exemplary tracking filter in accordance with another embodiment of the invention;

**[0008]** Figure 5 illustrates a schematic diagram of an exemplary switched capacitor array (CSA) in accordance with another embodiment of the invention;

**[0009]** Figure 6 illustrates a flow diagram of an exemplary method of calibrating a tracking filter in accordance with another embodiment of the invention;

**[0010]** Figure 7 illustrates a flow diagram of an exemplary method of tuning a tracking filter in accordance with another embodiment of the invention;

**[0011]** Figure 8 illustrates a flow diagram of an exemplary method of calibrating a tracking filter in accordance with another embodiment of the invention;

**[0012]** Figure 9 illustrates a flow diagram of an exemplary method of tuning a tracking filter in accordance with another embodiment of the invention;

**[0013]** Figure 10 illustrates a table depicting exemplary binary codes for the parallel and series capacitors of a tracking

filter corresponding to selected channels covered by the tracking filter;

**[0014]** Figure 11 is a circuit diagram for one embodiment of the preselect filter 202;

**[0015]** Figure 12 illustrates a block diagram of an exemplary tunable receiver in accordance with an embodiment of the invention having a baseband output; and,

**[0016]** Figure 13 illustrates a block diagram of an exemplary tunable receiver in accordance with an embodiment of the invention having a baseband digital output.

**[0017]** Figure 14 is a block diagram of an integrated circuit comprising a plurality of digitally programmable capacitor banks and the control therefore.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention tunable filters are ideal for use in tuners such as video tuners, and accordingly, preferred embodiments will be disclosed with respect to such tuners. It is to be understood, however, that the tunable filters, and the integrated capacitor banks useable in tunable circuits, may be used in many other applications.

### I. THE TUNABLE RECEIVER DESIGN

**[0018]** Figure 2 is a block diagram of an exemplary tunable receiver 200 in accordance with an embodiment of the invention. The tunable receiver 200 comprises a preselect filter 202, a first low noise amplifier (LNA) 204 having a controllable gain and an associated output power monitor device 206, a bank of selectable and digitally-tunable tracking filters 208, a second LNA 210, a harmonic and image reject down converting stage 212, an intermediate frequency (IF) trap 214, a first IF amplifier

216, an IF band pass filter (BPF) 218, and a second IF amplifier 220 having a controllable gain. In addition, the tunable receiver 220 comprises a synthesizer local oscillator (L.O.), a controller 224, a memory 226, and a control and data bus 228.

**[0019]** More specifically, details of an embodiment of the preselect filter 202 is shown in Figure 11. The circuit includes two on-chip spiral inductors, L0 and L1, two fixed capacitors, C0 and C1, two MOSFET switches, SW1 and SW2, and a two-state (1-bit) digitally tunable capacitor. An external inductor to ground is connected to the pin labeled "shunt_l_ext". When control bit "d" is high, the circuit acts as a high pass filter and when it is brought low, it acts as a UHF band stop filter, or essentially a low pass filter.

**[0020]** A reason for the use of the preselect filter 202 is to improve the linearity and the unwanted signal rejection characteristics of the tunable receiver 200. Specifically, rejecting a particular band at this stage substantially lowers the power level of the received RF signal at the input of the first LNA 204, thereby improving the linearity of the LNA 204 and other downstream elements of the tunable receiver 200. The unwanted signal rejection characteristics of the tunable receiver 200 is dependent on the linearity of the receiver. Accordingly, by improving the linearity of the receiver 200 through the use of the preselect filter 202, the unwanted signal rejection characteristics of the tunable receiver 200 is also improved.

**[0021]** Downstream of the preselect filter 202 is the first LNA 204 which provides a first stage of signal amplification for the tunable receiver 200. The first LNA 204 and accompanying circuitry, namely the directional coupler 205, power monitor

device 206, control and data bus 228, controller 224, and memory 226, are configured to maintain the first LNA 204 operating within a particular linearity specification. Specifically, the power monitor device 206, which is optional and may not always be included, may generate a parameter (e.g. a voltage) having a characteristic (e.g. an amplitude) related to the power level of the received RF signal at the output of the first LNA 204. If the controller 224 determines that the power monitor signal indicates that the power of the RF signal at the output of the first LNA 204 is at or above a pre-determined threshold, the controller 224 causes the gain of the first LNA 204 to reduce such that the power level is below the pre-determined threshold. Again, this feature improves the linearity of the tunable receiver 200, and consequently, improves the unwanted signal rejection characteristics of the tunable receiver 200.

**[0022]** Downstream of the first LNA 204 lies the bank of tracking filters 208 which are employed to provide rejection (i.e. suppression) of the image, harmonics, spurious, and other unwanted signals. More specifically, the bank of tracking filters 208 comprises a first controllable switch 238, a plurality of tracking filters 240, 242, 244, and 246, and a second controllable switches 250. The first controllable switches 238 comprise an input coupled to the output of the first LNA 204, a plurality of outputs coupled respectively to the plurality of tracking filters 240, 242, 244, and 246, and a controllable input which receives a control signal from the control and data bus 228 that controls the coupling between the switch input and any of the switch outputs. The second controllable switches 250 comprise a plurality of inputs coupled to the respective outputs of the tracking filters 240,

242, 244, and 246, an output coupled to the input of the second LNA 210, and a controllable input which receives control signals from the control and data bus 228 that controls the coupling between the switch output and either of the switch inputs.

**[0023]** The tracking filters 240, 242, 244, 246 are each configured to pass a distinct sub-band of channels, and substantially reject the remaining the undesired sub-bands of channels. For instance, tracking filter 240 may be configured to pass channels within a frequency sub-band extending from 50 to 150 MHz, tracking filter 242 may be configured to pass channels within a frequency sub-band extending from 150 to 350 MHz, tracking filter 244 may be configured to pass channels within a frequency sub-band extending from 350 to 650 MHz, and tracking filter 246 may be configured to pass channels within a frequency sub-band extending from 650 to 878 MHz. In addition, each of the tracking filters 240, 242, 244, and 246 may be digitally tunable to optimally pass a particular channel lying within the corresponding frequency sub-band, while rejecting the corresponding image signal, harmonics, spurious signals, and other unwanted signals. For example, the tracking filter 246 may be digitally tuned to optimally pass a 6 MHz width channel centered at 700 MHz, while substantially rejecting the image signals lying within the frequencies between 607 to 613 MHz and other undesired signals lying outside the intended channel of 697 to 703 MHz. In addition, by performing the undesired signal rejection, the tracking filter helps reduce the RF signal power for downstream elements to improve the linearity of the receiver 200. In some applications, more or fewer tracking filters may be used.

**[0024]** The controller 224, under the control of one or more software modules stored in the memory 226, may control the first and second controllable switches 238 and 250 by way of the control and data bus 228 to selectively couple the desired tracking filter in the path of the received RF signal. In addition, the controller 224, under the control of one or more software modules stored in the memory 226, may also digitally tune the selected tracking filter 242 by way of the control and data bus 228 to optimally pass the signals in the desired channel while rejecting the image signals, harmonics, spurious, and other unwanted signals lying outside of the desired channel. This will be discussed in more detail later with regard to a specific tracking filter implementation in accordance with the invention.

**[0025]** Downstream of the bank of tracking filters 208 lies another stage of signal amplification provided by the second LNA 210. The second LNA increases the power level of the received signal to compensate for losses incurred in the prior tracking filter stage. In addition, the second LNA 210 further converts the RF signal to a differential RF signal useful in the following down converting stage.

**[0026]** Downstream of the second LNA 210 lies the down converting stage 212 which converts the received RF signal to an intermediate frequency (IF) signal, while further rejecting the image, harmonics, spurious, and other unwanted signals residing outside of the desired channel. The down converting stage 212 comprises six (6) mixers each having a pair of inputs coupled to the differential outputs of the second LNA 210. The six (6) mixers also have inputs to respectively receive the different phases of the L.O. For instance, mixer 252 has an input to receive the L.O. signal cycling with a relative phase of zero

(0) degree, mixer 254 has an input to receive the L.O. signal cycling with a relative phase of -45 degrees, mixers 256 and 258 have respective inputs to receive the L.O. signal cycling with a relative phase of -90 degrees, mixer 260 has an input to receive the L.O. signal cycling with a relative phase of -135 degrees, and mixer 262 has an input to receive the L.O. signal cycling with a relative phase of -180 degrees. The differential outputs of mixers 252, 254, and 256 are coupled together and applied to a 90 degree phase shifter 264 whose differential outputs, in turn, are coupled to a first input of a summing device 266. The differential outputs of mixers 258, 260, and 262 are coupled together and applied to the second input of the summing device 266. Alternatively, the 90 degree phase shifter 264 and the summing device 266 may be replaced with a polyphase filter.

**[0027]** In a typical conventional image rejection mixer, two mixers are used, both being driven by the local oscillator frequency, but at a 90 degree phase shift with respect to each other. The mixers both generate outputs of sum and difference frequency components which themselves are 90 out of phase with respect to each other. Then one of the mixer outputs is shifted 90 degrees and the two outputs are then combined (added together). Now, depending on selection of the location and direction of the 90 degree phase shifts, either the sum frequency components of the two mixer outputs add (are equal and inphase with each other) and the difference frequency components subtract (are equal and 180 degrees out of phase with each other), or the difference frequency components of the two mixer outputs add and the sum frequency components subtract, thereby passing the sum or difference frequencies, as

desired, and eliminating (grossly attenuating) the difference or sum frequencies, respectively.

**[0028]** In a typical mixer, the signal is multiplied not by a sine wave, but rather multiplied by a square wave. This creates harmonics of the desired frequency band, with negative effects on linearity and range of subsequent circuitry. In the image rejection mixer of Figure 2, four additional mixers are included, each operated at additional phase shifts as shown. The additional mixers have the effect of eliminating certain harmonics from the image rejection mixer output, avoiding problems caused by such harmonics.

**[0029]** Downstream of the down converting stage 212 lies the IF trap 214 which is provided to remove undesired signals generated by the down converting stage 212, to reduce the number of channels in the IF signal, and to reduce the power level of the IF signal to improve the linearity of downstream stages. The IF trap 214 is coupled across the differential signals at the output of the summing device 266. The IF trap 214 comprises a series resonant circuit coupled across the differential signal lines at the output of the summing device 266.

**[0030]** Downstream of the IF trap 214 lies a first stage of IF signal amplification provided by the IF amplifier 216 to compensate for signal losses incurred in the down converting stage 212, and losses that will be incurred in the following IF filter stage. The IF amplifier 216 comprises a pair of differential signal inputs coupled respectively to the differential signal outputs of the summing device 266. The IF amplifier 216 also comprises differential signal outputs.

**[0031]** Downstream of the first IF amplifier 216 lies the IF band pass filter (BPF) 218 which performs the channel select

filtering for the tunable receiver 200. The IF BPF 218 is configured to perform high rejection of undesired signals lying outside of the selected channel.

**[0032]** Downstream of the IF BPF 218 lies a second stage of IF signal amplification provided by the second IF amplifier 220 to compensate for losses in the IF signal incurred in the filtering of the signal by the IF BPF 218. The IF amplifier 220 includes differential signal inputs coupled to the differential signal outputs of the IF BPF 218. The output IF signal of the selected channel is generated at the differential signal outputs of the IF amplifier 220. The IF amplifier 220 further comprises a gain control input coupled to the control and data bus 228 for controlling the gain of the IF amplifier 220. This allows the gain of the IF amplifier 220 to be controlled so that the power level of the output IF signal is regulated.

**[0033]** The synthesizer L.O. 222 generates the L.O. with the appropriate phases zero (0), -45, -90, -135, and -180 degrees for use by the down converting stage 212. The controller 224, under the control of one or more software modules stored in the memory 226 and an external controller, can control the synthesizer L.O. 222 by way of the control and data bus 228 to generate the appropriate frequency based on the selected channel. The controller 224 receives instructions from an external controller, and performs the intended operations under the control of one or more software modules stored in memory 226.

**[0034]** In operation, the controller 224 may receive an instruction from the external controller to tune the tunable receiver 200 to receive a particular channel. In response, the controller 224, under the control of one or more software

modules stored in the memory 226, issues instructions to set the switches in the preselect filter 202 in the path of the received RF signal to select the desired band of channels. Also in response, the controller 224, under the control of one or more software modules stored in the memory 226, issues instructions to the switches 238 and 250 to couple the appropriate tracking filter 240, 242, 244 or 246 in the path of the received RF signal. In addition, the controller 224, under the control of the one or more software modules stored in the memory 226, digitally tunes the selected tracking filter to optimize the passing of the selected channel while substantially rejecting the image and other unwanted signals. Also in response to the channel-select command received from the external controller, the controller 224, under the control of one or more software modules stored in the memory 226, issues instructions to the synthesizer L.O. 222 to generate the L.O. signal with the appropriate frequency and phases for the selected channel.

**[0035]** In addition, the controller 224 may also receive commands from the external controller to adjust the gain of the first LNA 204 and the second IF amplifier 220. For instance, the output of the power monitor device 206 may be provided to the external controller either directly or by way of the controller 224 and control and data bus 228. If the output of the power monitor device 206 indicates that the power level of the RF signal at the output of the first LNA 204 is at or above a pre-determined threshold, the external controller may send a command to the controller 224 to lower the gain of the first LNA 204. In response, the controller 224, under the control of the one or more software modules stored in the memory 226, issues an instruction to the first LNA 204 by way of the

control and data bus 228 to lower its gain so that the power level of the RF signal at the output of the first LNA 204 is below the pre-determined threshold.

**[0036]** Similarly, if the external controller deems that the power level of the IF output signal is not within specification, the external controller issues a command to the controller 224 to adjust the gain of the second IF amplifier 220. In response, the controller 224, under the control of one or more software modules stored in the memory 226, issues an instruction to the second IF amplifier 204 by way of the control and data bus 228 to adjust its gain such that the power level of the output IF signal is within specification.

## II. THE TRACKING FILTER DESIGN

**[0037]** Figure 3 illustrates a schematic diagram of an exemplary tracking filter 300 in accordance with another embodiment of the invention. The tracking filter 300 is one example of a tracking filter that can be used as any one of the tracking filters 240, 242, 244, and 246 of the tunable receiver 200. The exemplary tracking filter 300 is a one resonator version of the filter. It comprises a capacitor Cseries connected in series with an inductor Lseries between input and output terminals of the filter 300. The tracking filter 300 further comprises a capacitor Cparallel connected in parallel with both the series capacitor Cseries and inductor Lseries. Additionally, the tracking filter 300 comprises a first shunt capacitor Cshunt1 connected between the input and a ground terminal and a second shunt capacitor Cshunt2 connected between the output and a ground terminal.

**[0038]** Both the series capacitor Cseries and the parallel capacitor Cparallel are variable, i.e. their capacitance can be

selected. As will be discussed in more detail later, the series and parallel capacitors each use a switched capacitor array for setting the desired capacitance of the capacitors. The series capacitor Cseries is used to set the frequency response of the pass band, i.e. the selected channel. As customary, it is desirable to minimize the insertion loss and maximize the return loss of the tracking filter for the pass band. The parallel capacitor Cparallel sets the frequency response of the image band. As customary, it is desirable to maximize the insertion loss of the tracking filter for the image band.

**[0039]** Figure 4 illustrates a schematic diagram of an exemplary tracking filter 400 in accordance with another embodiment of the invention. The tracking filter 400 is similar to track filter 300, except that filter 400 includes an additional resonator being the mirror image of the first resonator and having Cshunt2 in common. More specifically, the tracking filter 400 comprises a first series capacitor Cseries connected in series with a first series inductor Lseries between the input and an intermediate node. The tracking filter 400 further comprises a first parallel capacitor Cparallel connected between the input and the intermediate node, i.e. in parallel with the first series capacitor Cseries and first series inductor Lseries.

**[0040]** In addition, the tracking filter 400 further comprises a second series inductor Lseries connected in series with a second series capacitor Cseries between the intermediate node and the output. Also, the tracking filter 400 comprises a second parallel capacitor Cparallel connected between the intermediate node and the output, i.e. in parallel with the second series capacitor Cseries and the second series inductor

Lseries. Further, the tracking filter 400 comprises an input shunt capacitor Cshunt1 connected between the input and a ground terminal, an intermediate shunt capacitor Cshunt2 connected between the intermediate node and a ground terminal, and an output shunt capacitor Cshunt1 connected between the output and a ground terminal.

**[0041]** Similar to the tracking filter 300, the first and second series capacitors Cseries and the first and second parallel capacitors Cparallel are variable, i.e. their capacitance can be selected. As will be discussed in more detail later, the series and parallel capacitors each use a switched capacitor array for setting the desired capacitance of the capacitors. The first and second series capacitor Cseries is used to set the frequency response of the pass band, i.e. the selected channel. As customary, it is desirable to minimize the insertion loss and maximize the return loss of the tracking filter for the pass band. The parallel capacitor Cparallel sets the frequency response of the image band. As customary, it is desirable to maximize the insertion loss of the tracking filter for the image band.

**[0042]** Figure 5 illustrates a schematic diagram of an exemplary switched capacitor array (CSA) 500 in accordance with another embodiment of the invention. As discussed above, the CSA 500 can be used as the series and parallel capacitors of the tracking filters 300 and 400. The exemplary switched capacitor array 500 is a six (6) bit binary weighted CSA. Accordingly, the CSA 500 comprises six (6) selectable capacitor banks 502-0 through 502-5 coupled in parallel to each other and across common nodes A and B. The selectable capacitor banks 502-0 through 502-5 are respectively selectable by way of select lines D0-5.

**[0043]** Each of the capacitor banks comprises a series path extending from node A to node B including a first capacitor, a switching device such as field effect transistor (FET) Q, and a second capacitor. For instance, the series path of capacitor bank 502-0 comprises first capacitor C, the channel of FET Q, and second capacitor C; the series path of capacitor bank 502-1 comprises first capacitor 2C, the channel of FET Q, and second capacitor 2C; the series path of capacitor bank 502-2 comprises first capacitor 4C, the channel of FET Q, and second capacitor 4C; the series path of capacitor bank 502-3 comprises first capacitor 8C, the channel of FET Q, and second capacitor 8C; the series path of capacitor bank 502-4 comprises first capacitor 16C, the channel of FET Q, and second capacitor 16C; and the series path of capacitor bank 502-5 comprises first capacitor 32C, the channel of FET Q, and second capacitor 32C.

The gates of the FETs of the capacitor banks 502-0 through 502-5 are respectively coupled to the select lines D0-5 by way of resistors R. The sources and the drains of the FETs of the capacitor banks 502-0 and 502-5 are respectively coupled to the select lines D0-5 by way of resistors R and inverters I.

**[0044]** In operation, when a desired capacitor bank is to be selected, the signal on the corresponding select line is driven to a logic high state (e.g. +3 Volts). Accordingly, the voltage on the gate of the FET is also approximately at the logic high level. The corresponding inverter I generates a logic low state (e.g. 0 Volt) in response to the corresponding select line being driven to a logic high state. This results in a logic low voltage (e.g. 0 Volt) present on the drain and source of the corresponding FET. The low logic voltage (e.g. 0 Volt) on the drain and source of the FET and the high logic voltage (e.g. +3 Volts) on the gate of the FET places the FET

in a low impedance mode, thereby electrically connecting the first and second capacitors in series between nodes A and B, and thus enabling the corresponding capacitor bank.

**[0045]** When a desired capacitor bank is to be deselected, the signal on the corresponding select line is driven to a logic low state (e.g. +0 Volt). Accordingly, the voltage on the gate of the FET is also approximately at the logic low level. The corresponding inverter I generates a logic high state (e.g. +3 Volts) in response to the corresponding select line being driven to a logic low state. This results in a logic high voltage (e.g. +3 Volts) present on the drain and source of the corresponding FET. The high logic voltage (e.g. +3 Volts) on the drain and source of the FET and the low logic voltage (e.g. 0 Volt) on the gate of the FET places the FET in a high impedance and low capacitance, thereby electrically isolating the first and second capacitors in series between nodes A and B, and thus disabling the corresponding capacitor bank.

**[0046]** The capacitor banks 502-0 through 502-5 of the exemplary CSA 500 provide a selectable binary weighted capacitance. For instance, capacitor bank 502-0 when selected provides an effective capacitance of approximately ½ C between nodes A and B, capacitor bank 502-1 when selected provides an effective capacitance of approximately C between nodes A and B, capacitor bank 502-2 when selected provides an effective capacitance of approximately 2C between nodes A and B, capacitor bank 502-3 when selected provides an effective capacitance of approximately 4C between nodes A and B, capacitor bank 502-4 when selected provides an effective capacitance of approximately 8C between nodes A and B, and capacitor bank 502-5 when selected provides an effective capacitance of 16C between nodes A and B. Thus, the overall capacitance provided

by the CSA 500 depends on the unique combination of selected capacitor banks 502-0 and 502-5.

## III. METHOD OF CALIBRATING AND TUNING THE TRACKING FILTER

**[0047]** As discussed in Section I regarding the design of the tunable receiver 200, the tracking filter may be employed to pass signals in the desired channel with minimal insertion loss, and to reject signals in the image band with maximum insertion loss. In addition, since a tracking filter covers a sub-band made up of a plurality of channels, the tracking filter is electronically tunable to minimize the insertion loss and maximize the return loss for the desired channel, and maximize the insertion loss for the image band. As discussed in Section II regarding the design of the tracking filter, the CSA are employed within a tracking filter to electronically adjust the capacitance of the series and parallel capacitors in order to achieve the desired frequency response for the selected channel band and for the image band. The following describes unique methods of calibrating and tuning a tracking filter in order to achieve these objectives.

**[0048]** Figure 6 illustrates a flow diagram of an exemplary method 600 of calibrating a tracking filter in accordance with another embodiment of the invention. According to the method 600, a measurement is taken of the frequency response of the pass and image bands of the tracking filter at the lowest frequency channel of the corresponding sub-band (block 602). Then, the codes on the select lines corresponding to the parallel and series capacitors of the tracking filters are adjusted to optimize the filter to provide the desired specification for the pass and image bands of the tracking filter (block 604). For example, such codes may be respectively a binary 27 and a

binary 63 for a lowest frequency channel centered at 570 MHz (See Figure 10). In a preferred embodiment, a nominal or most probable code is determined, and the difference between the optimal code and the nominal code for that IC is written into memory 226 of the tunable receiver 200 for use by the controller 224 in tuning the tracking filter (block 606).

**[0049]** After the codes corresponding to the lowest frequency channel have been determined, a measurement is taken of the frequency response of the pass and image bands of the tracking filter at the highest frequency channel of the corresponding sub-band (block 608). Then, the codes on the select lines corresponding to the parallel and series capacitors of the tracking filter are adjusted to optimize the filter to provide the desired specification for the pass and image bands of the tracking filter (block 610). For example, such codes may be respectively a binary 4 and a binary 1 for a highest frequency channel centered at 820 MHz (See Figure 10). After such codes have been determined, in the preferred embodiment, the difference between the optimal code and the nominal code for that IC are written into memory 226 of the tunable receiver 200 for use by the controller 224 in tuning the tracking filter (block 612).

**[0050]** Figure 7 illustrates a flow diagram of an exemplary method 700 of tuning a tracking filter in accordance with another embodiment of the invention. According to the method 700, the controller 224 receives a command from an external controller to tune the receiver to a selected channel (block 702). The controller 224 then determines which tracking filter 240, 242, 244, or 246 covers the selected channel and instructs the switches 238 and 250 to couple the selected tracking filter in the path of the received RF signal (block 704). Then, the

controller 224 performs an appropriate (possibly nonlinear) interpolation to determine the code for the parallel capacitor of the corresponding tracking filter (block 706).

**[0051]** Then, the controller 224 performs another predetermined (possibly nonlinear) interpolation to determine the code for the series capacitor of the corresponding tracking filter (block 708). After the controller 224 determines the codes for the parallel and series capacitors, the controller 224 sends the codes to the corresponding tracking filter by way of the control and data bus 228 (block 710).

**[0052]** Figure 8 illustrates a flow diagram of an exemplary method 800 of calibrating a tracking filter in accordance with another embodiment of the invention. According to the method 800, a measurement of the frequency response of the pass band and image band of the tracking filter is taken at a selected channel (block 802). Then, the codes on the select lines for the series and parallel capacitors are adjusted to achieve a desired frequency response for the pass band and image band of the tracking filter for the selected channel (block 804). The codes are then written into the memory 226 in a look-up table structure or the like for use by the controller 224 in tuning the corresponding tracking filter (block 806). At this point, it is determined whether the codes for all the channels covered by the corresponding tracking filter have been determined (block 808). If they have not, then the selected channel is changed to a channel in which the codes have yet to be determined (block 810), and the method 800 proceeds back to block 802. Otherwise, the method 800 of calibrating the tracking filter is complete.

**[0053]** Figure 9 illustrates a flow diagram of an exemplary method of tuning a tracking filter in accordance with another

embodiment of the invention. According to the method 900, the controller 224 receives a command from an external controller to tune the receiver to a selected channel (block 902). The controller 224 then determines which tracking filter 240, 242, 244, or 246 covers the selected channel and instructs the switches 238 and 250 to couple that tracking filter in the path of the received RF signal (block 904). Then, the controller 224 performs a look-up in a table-like data structure (see Figure 10) stored in the memory 226 and reads the corresponding codes for the parallel and series capacitors (block 906). Referring to Figure 10, if, for example, the selected channel is centered at 760 MHz, the controller 224 merely reads the binary codes associated with that channel, such as binary code 10 for the parallel capacitor and binary code 6 for the series capacitor. After the codes have been read, the controller 224 sends them to the tracking filter by way of the control and data bus 228 (block 908).

**[0054]** Now referring to Figure 12, an alternate embodiment of the present invention may be seen. This embodiment may be substantially identical to the embodiment of Figure 2 with the exception that the output of the low noise amplifier 210 is converted directly to baseband. Because of the conversion to baseband, there are no image frequencies to worry about and accordingly, a simple I-Q demodulator or converter may be used. The references for mixers 272 and 274 are provided by local oscillator 276 driven by synthesizer 270 controlled through the bus 228, the two mixers 272 and 274 being driven by the local oscillator 90 degrees out of phase with each other to provide the in-phase and quadrature outputs. These outputs in turn are amplified by amplifiers 278 and 280 and filtered by low pass filters 282 and 284 to provide the I and Q outputs through

variable gain amplifiers 286 and 288. Alternatively, the mixers 272 and 274 may be harmonic rejection mixers of the general type illustrated wit respect to the embodiment of Figure 2.

**[0055]** A still further embodiment is shown in Figure 13. This embodiment is very similar to the embodiment of Figure 12, though with the baseband signals being provided as digital outputs. Thus, in this embodiment, the outputs of variable gain amplifiers 286 and 288 are provided to one-bit sigma-delta converters or modulators 290 and 292 and each converted to a low voltage differential signal by the LVDS interfaces 294 and 296. In this embodiment, the sigma-delta modulators provide an automatic gain control signal for the variable gain amplifiers 286 and 288. The local oscillator 296 also provides a timing reference for the low voltage digital signal outputs. Alternatively, other analog to digital conversion technologies may be used, such as, by way of example, pipelined analog to digital converters, in place of the sigma-delta converters 290 and 292.

**[0056]** Tunable filters in general may use all discrete inductors, such as surface mount and/or as printed on a printed circuit board. As such, tuning of such a filter may be advantageously done by using integrated capacitor banks switchable under digital control. Figure 14 is a block diagram of such an integrated circuit. The m + 1 capacitor banks CSA0 through CSAm may each be in accordance with Figure 5, each bank having n + 1 capacitances in a binary progression, individually switchable to a respective one of the m + 1 capacitor bank outputs A0,B0 through Am,Bm. The control may simply be a shift register into which a control word may be serially loaded, with each bit controlling a respective capacitor switch. The

control may also take other forms, such as, by way of example, that of Figures 2, 12 and 13, wherein a controller and memory are included. A serial interface to the controller is still preferred over a parallel interface to reduce the pin count, but the controller and memory allows the storage of calibration data as well as a control word, so that the controller may receive any of a plurality of predetermined control words and control the capacitor switches responsive to each control word and the respective calibration data.

**[0057]** The capacitor banks CSA0 through CSAm may also take other forms. By way of example, referring to both Figures 5 and 14, each capacitor bank may be comprised of n + 1 capacitance values in a binary progression, each capacitance value comprising a single capacitor in series with a MOS switch, each series combination for each bank being coupled to the respective A and B lines. Further, in some circuits that could use digitally programmable integrated capacitor banks of this general kind, at least some of the capacitors have a common lead, typically the circuit ground. Consequently at least some, perhaps half the number of capacitor banks, could have a common lead A or B.

**[0058]** The level of integration of the digitally tunable filters of the present invention may vary as desired. By way of example, one or more of the inductors may be surface mount inductors, with the rest of the digitally tunable filter circuit incorporated in or as part of a single integrated circuit. Similarly, while the capacitors of the switched capacitor array of Figure 5 are switchable in circuit individually or in parallel, switched capacitor arrays allowing switching the capacitors in series may also be used. One or more of the inductors of the digitally tunable filter may be realized as a printed inductor on the LGA (land grid array) package, with the

other inductor or inductors realized on-chip, so that the entire digitally tunable filter, alone or as part of a larger integrated circuit, is provided in a single plastic package. Similarly, one or more of the inductors may be printed inductors on a printed circuit board and one or more of the inductors may be surface mount inductors attached to the printed circuit board, with the rest of the digitally tunable filter circuit incorporated in the single integrated circuit.

**[0059]** In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will be evident however, that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.